Midterm Exam

(October 19th @ 3:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (22 PTS)

a) Complete the following table. The decimal numbers are unsigned: (3 pts.)

Decimal	BCD	Binary	Reflective Gray Code
			101010
		01000101	

b) Complete the following table. Use the fewest number of bits in each case: (15 pts.)

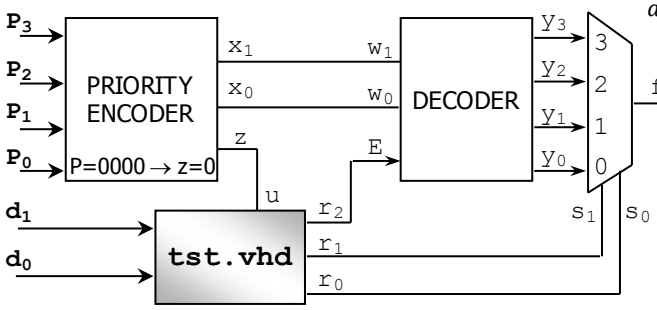
REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
	110011		
		11111	
			1000
		011101	
-16			
			101000

c) Convert the following decimal numbers to their 2's complement representations. (4 pts.)

✓ -16.5 ✓ 18.75

PROBLEM 2 (14 PTS)

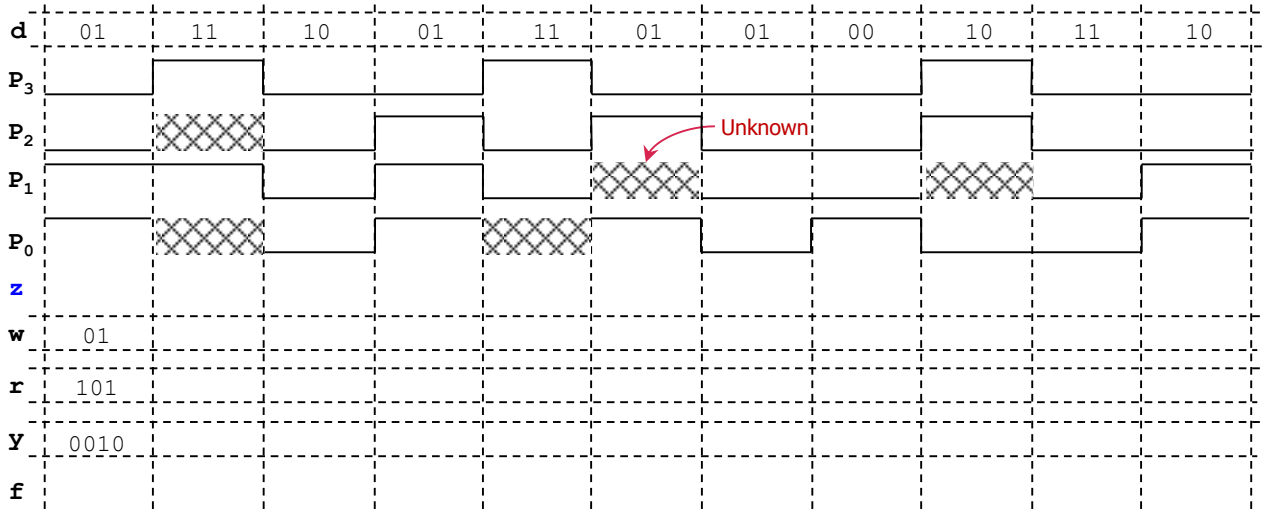
- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.



$d = d_1 d_0$, $w = w_1 w_0$, $r = r_2 r_1 r_0$, $y = y_3 y_2 y_1 y_0$

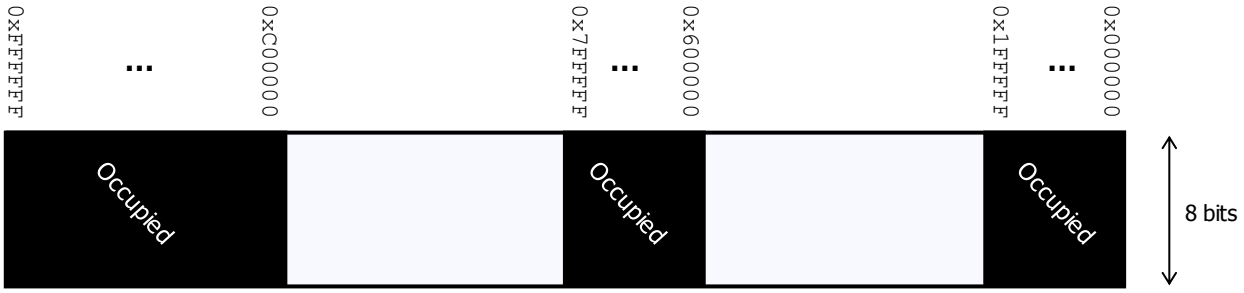
```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= d&'0';
     if u = '1' then
        r <= '1'&d;
     end if;

  end process;

end bhv;
```



PROBLEM 3 (12 PTS)

- The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte. 1KB = 2^{10} bytes, 1MB = 2^{20} bytes, 1GB = 2^{30} bytes
  - ✓ What is the size (in bytes, KB, or MB) of the memory space? What is the address bus size of the microprocessor? (3 pts.)
  - ✓ If we have a memory chip of 2 MB, how many bits do we require to address those 2 MB of memory? (1 pt.)
  - ✓ We want to connect the 2 MB memory chip to the microprocessor. For optimal implementation, we must place those 2 MB in an address range where every single address shares some MSBs. Provide a list of all the possible address ranges that the 2 MB chip can occupy. You can only use the non-occupied portions of the memory space as shown below.



PROBLEM 4 (17 PTS)

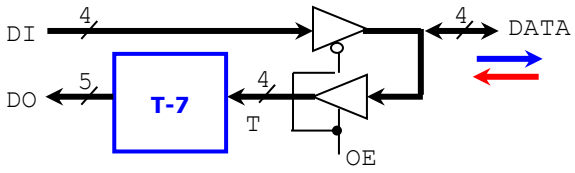
a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher bit. (6 pts.)
   - ✓ `29 - 51`
   - ✓ `29 + 51`

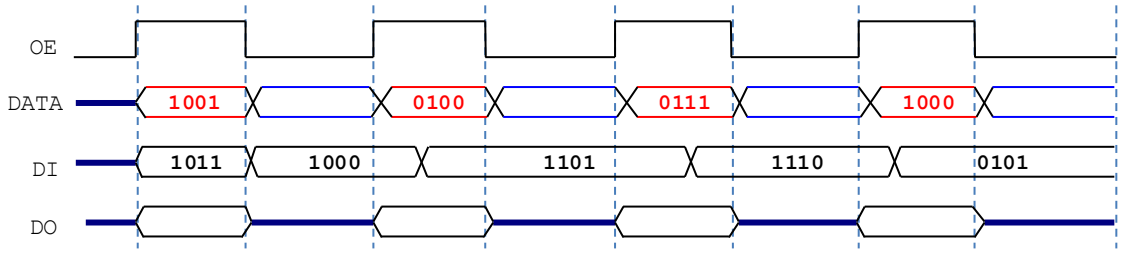
b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts.)
   - ✓ `29 - 51`
   - ✓ `-53 - 26`

c) Get the multiplication result of the following numbers that are represented in 2's complement arithmetic with 4 bits. (3 pts.)
   - ✓ `-5 x 7`

PROBLEM 5 (11 PTS)

- Complete the timing diagram (signals DO and $DATA$) of the following circuit. The circuit in the blue box computes the signed operation T-7, with the result having 5 bits. T is a 4-bit signed (2C) number.
  - ✓ Example: if T=1010:
    DO = 1010 - 0111 = 11010 + 11001
    DO = 10011





PROBLEM 6 (10 PTS)

- Sketch the circuit that computes $|A - B|$, where A, B are 4-bit unsigned numbers. For example, $A = 0101, B = 1101 \rightarrow |A - B| = |5 - 13| = 8$. You can only use full adders (or multi-bit adders) and logic gates. Your circuit must avoid overflow: design your circuit so that the result and intermediate operations have the proper number of bits.

PROBLEM 7 (14 PTS)

- Given the following Boolean function: $f(x, y, z) = \prod M(3,4)$
  a) Provide the simplified expression for f and sketch this circuit using logic gates. (4 pts)
  b) Implement the previous circuit using ONLY 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (10 pts)